WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

an insulating substrate;

a first signal wire formed on the insulating substrate;

a second signal wire formed on the insulating substrate and intersecting the first signal wire in an insulating manner;

first and second pixel electrodes formed in a pixel area defined by the intersections of the first and the second signal wires and including a plurality of subareas partitioned by cutouts;

a direction control electrode formed in the pixel area and including a portion overlapping at least one of the cutouts; and

a first thin film transistor connected to the direction control electrode, the first signal wire, and the second signal wire.

2. The thin film transistor array panel of claim 1, further comprising:

a second thin film transistor connected to the first pixel electrode, the first signal wire, and the second signal wire.

3. The thin film transistor array panel of claim 2, further comprising:

a third thin film transistor connected to the first pixel electrode, the first signal wire, and the second signal wire.

4. The thin film transistor array panel of claim 3, wherein the first signal wire includes first and second signal lines, the second signal wire includes third and fourth signal lines, the second thin film transistor is connected to the first signal line, the third signal line,

and the first pixel electrode, the third thin film transistor is connected to the second signal line, the third signal line, and the first pixel electrode, and the first thin film transistor is connected to the second signal line, the fourth signal line, and the direction control electrode.

5. The thin film transistor array panel of claim 3, further comprising a third signal wire intersecting the second signal wire in an insulating manner.

6. The thin film transistor array panel of claim 5, wherein the first signal wire includes first and second signal lines, the second signal wire includes third and fourth signal lines, the second thin film transistor is connected to the first signal line, the third signal line, and the first pixel electrode, the third thin film transistor is connected to the second signal line, the third signal line, and the first pixel electrode, and the first thin film transistor is connected to the second signal line, the third signal wire, and the direction control electrode.

7. The thin film transistor array panel of claim 5, wherein the first signal wire includes first and second signal lines, the second signal wire includes third and fourth signal lines, the second thin film transistor is connected to the first signal line, the third signal line, and the first pixel electrode, the third thin film transistor is connected to the second signal line, the third signal wire, and the first pixel electrode, and the first thin film transistor is connected to the second signal line, the fourth signal line, and the direction control electrode.

8. The thin film transistor array panel of claim 1, further comprising a coupling electrode connected to the first pixel electrode and overlapping at least one of the cutouts of the second pixel electrode, wherein the direction control electrode includes a portion overlapping one of the cutouts of the first pixel electrode and does not overlap the

cutouts of the second pixel electrode.

9. The thin film transistor array panel of claim 1, wherein the direction control electrode overlaps the cutouts of the first and the second pixel electrodes.

10. The thin film transistor array panel of claim 1, wherein the cutouts of the second pixel electrode comprise a transverse cutout bisecting the second pixel electrode into upper and lower halves and a plurality of first oblique cutouts having inversion symmetry with respect to the transverse cutout, and the cutouts of the first pixel electrode comprise a plurality of second oblique cutouts having inversion symmetry with respect to the transverse cutout.

11. The thin film transistor array panel of claim 10, wherein the first and the second pixel electrodes have inversion symmetry with respect to the transverse cutout.

12. The thin film transistor array panel of claim 10, further comprising a third signal wire intersecting the second signal wire in an insulating manner and including an electrode disposed between the first pixel electrode and the second pixel electrode.